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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,409	07/18/2003	I-TSENG LEE	10672-US-PA	1408

31561 7590 09/21/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
HA, NATHAN W	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,409	LEE ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Cancellation of claim 3 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, and 6-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art, AAPA, Fig. 1, and in view of Chen et al. (US 2002/0096754, newly cited, hereinafter, Chen.)

In regard to claims 1-2, 7-8, 12-13, and 18, in fig. 1 and pp. 2-4, the AAPA discloses a stack chip package structure, comprising:

a carrier 110, section [0007], line 5, or die pad (col.6, line 28) with a carrier surface and a back surface, wherein the bonding pads 114, section [0007], line 10, are set up on the carrier surface where the wires 150 are connected thereto (section [0007], line 6);

a die 120 (section [0007], line 5) with an active surface and a back surface, wherein the back surface of the die is in contact with the carrier surface of the carrier and the active surface of the die has a plurality of metal pads 12 thereon (col.6, lines 4-6);

an adhesive layer 142 (section [0007], line 15) on the active surface of the die;

a thermal conductive block 130, section [0007], line 17, with a bonding surface for attaching to the active surface of the die through the adhesive layer, wherein the adhesive layer between at least one of the peripheral surfaces and the active surface of the die is thicker than the adhesive layer between the central surface and the active surface;

a plurality of conductive wires 150 electrically connecting each metal pad to a corresponding bonding pad; and

a molding compound 160 enclosing the die, the thermal conductive block and the conductive wires (section [0007], line 24).

The AAPA, however, does not expressly disclose that the peripheral includes surfaces that are surrounding the central surface.

Chen, in fig. 3, discloses an analogous semiconductor package including a carrier 22, a chip 34, and another chip which can be considered as a thermal conductive block, bond wires 44. Chen further discloses that the central surface is being surrounding by peripheral surfaces created by recesses 51, ladder shape as claimed in claims 2 and 8. These recesses prevent the damage and press to the bond wires from upper devices. See also, [0025] and [0031].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to create recesses as taught by Chen in the

AAPA's device in order to protect the bond wires from damage by pressing in a stack structure.

It should be noted that the element 46 is considered as a thermal block since most materials are capable of delivering heat, or conducting heat.

In regard to claims 4 and 19, Chen further discloses wherein the carrier is a substrate (section [0022], line 1). Also, the element 110 in the AAPA functions as a carrier of the stack structure.

In regard to claims 6, 11, and 15, the AAPA further discloses that the thermal conductive block is a dummy die or metallic (AAPA's [0007], lines 16-17.)

In regard to claim 9, the AAPA discloses the molding compound exposes the back surface of the die. See AAPA's fig. 1.

In regard to claims 10 and 14, see above discussions regarding to claim 1, wherein the thickness of the outer adhesive is thicker than the inner area. See also fig. 1 of the AAPA, and fig. 3, of Chen.

In regard to claim 16, see above discussions regarding to claim 1, wherein the stack includes the thermal block.

In regard to claim 17, IC or chip 120 is also a functional IC device, where the upper surface includes electrical pads, which connect to the upper device by bond wires.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA and Chen as applied to claims 1-2, 4, and 6-19 above and further in view of Nakaoka et al. (US 2003/0127722, newly cited, hereinafter, Nakaoka.)

In regard to claim 5, the above combination of the AAPA and Chen discloses all of the claimed limitations except that the carrier is a lead frame having leads for attaching conductive wires.

Nakaoka, in fig. 3, Chen discloses an analogous structure, a stack chip package structure, comprising:

a carrier 22, or substrate (section [0022]), with a carrier surface and a plurality of bonding pads 26 (section [0022]), or signal terminal, wherein the bonding pads are set up on the carrier surface;

a die 34 (or IC die, section [0023], line 1) with an active surface and a back surface (or lower and upper surfaces 36 and 38, respectively, section [0023], lines 1-3), wherein the back surface of the die is in contact with the carrier surface of the carrier and the active surface of the die has a plurality of metal pads 42 formed thereon (or bonding pad, section [0024], line 3);

an adhesive layer 52 on the active surface of the die (section [0025], line 6);

a thermal conductive block 136 with a bonding surface for attaching to the active surface of the die through the adhesive layer 132, wherein the bonding surface includes a central surface and a plurality of peripheral surfaces surrounding the central surface, wherein the peripheral surfaces are further away from the active surface of the die than the central surface relatively, and that the peripheral surfaces and the central surface are on non-coplanar planes;

a plurality of conductive wires 112A electrically connecting each metal pad to a corresponding bonding pad; and a molding compound enclosing the die, the thermal conductive block and the conductive wires. Nakaoka further discloses that the carrier is a lead frame having a plurality of leads having a bonding pad on the lead for attaching conductive wires 35, section [0081]. It should be noted that lead frame is widely used in semiconductor packaging as a common carrier substrate. It can be used to substitute with the regular carrier as disclosed by Chen, for example, in order to eliminate solder ball connections at the bottom of the substrate. This structure makes it easier to attach the package to the substrate since the solder can be done on the sides of the package.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute a lead frame as taught by Nakaoka in the AAPA and Chen's combination in order to eliminate solder ball connections at the bottom of the substrate. This structure makes it easier to attach the package to the substrate since the solder can be done on the sides of the package.

Response to Arguments

4. Applicant's arguments with respect to claims 1-2 and 4-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha
September 15, 2004